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To Study Effect on Current Due to Channel Length Variation

Abneesh Kumar [a, *], Atal Rai [a], R. K. Saxena [b], Suresh Patel [c]
[a] Department of Electronic and Compunction Engineering, IIMT Engineering College, Meerut, Uttar Pradesh, India
[b] Department of Electronics Instrumentation and Control Engineering, Institute of Engineering & Technology, Alwar, India
[c] J.T.O BSNL, Jamnagar, Gujarat, India

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Abstract
There are two primary device structures that have being widely used. One is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate. The other one is called SOI (silicon-on-insulator), where a transistor is built on a thin silicon layer, which is separated from the substrate by a layer of insulator or device scaling; it is basically try to balance two things: device functionality and device reliability. Both of them have to be maintained at a smaller dimensional size [1]. In this paper, three transistors are proposed having different channel lengths 8 micron, 16 micron and 24 micron. Simulation shows that with a fixed gate length, when channel length is increased, the output characteristics slope is decreased.

1. Introduction

According to Moore's law, The dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years, Traditional Silicon based MOSFET (Metal Oxide Transistor Field effect transistor) gives the better performance [2]. The threshold voltage of a long channel device is independent of the channel length and the drain voltage. It is depend on the body bias. However, as the channel length becomes shorter and shorter, the threshold voltage shows a greater dependence on the channel length and the drain voltage. The dependence of the threshold voltage on the body bias becomes weaker as channel length becomes shorter, because the body bias has less control of the depletion region. Short-channel effects must be included in the threshold voltage in order to model deep-submicron devices correctly [3].

2. Calculation for MOSFET Geometry

Consider a cross section view of MOSFET as shown in the fig-(1). The channel length and width is calculated as

$LE = L - \Delta L = L + \Delta LPS - 2.\ \Delta Loverlap$ (1)

$WE = W - \Delta W = W + \Delta WOD - 2.\ \Delta Wnarrow$ (2)

Where L_{PS} = Difference between the actual and the programmed silicon gate length

$\Delta L_{overlap}$ = Effective channel length reduction per side due to the lateral diffusion of the source/drain dopant ions

L = Drawn channel length of the actual transistor

W = Drawn channel width in the lay-out of the actual transistor

ΔW_{OD} = Difference between the actual and the programmed field–oxide opening

ΔW_{narrow} = Effective reduction of the channel width per side due to the lateral diffusion of the channel–stop dopant ions

The LE and WE after calculation should not be less than 0.

3. Discussion & Result

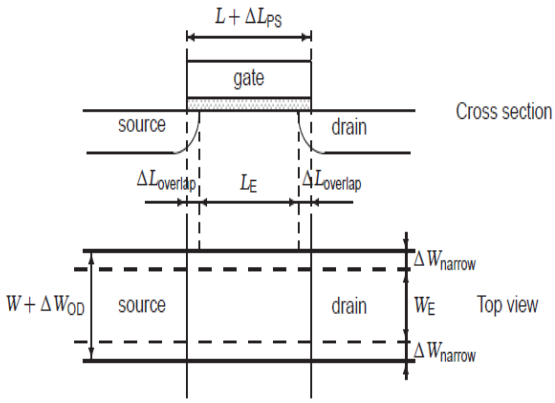

Fig: 1. Cross Section View of MOSFET

The short channel effects on the threshold voltage by considering the parameters shown in the fig-2. The source and drain are characterized by a diffused junction depth $r_{j..}$ Assume that the lateral diffusion distance under the gate is same as the vertical diffused distance. This assumption is good approximation for diffused junction but becomes less accurate for ion implemented junctions [5].

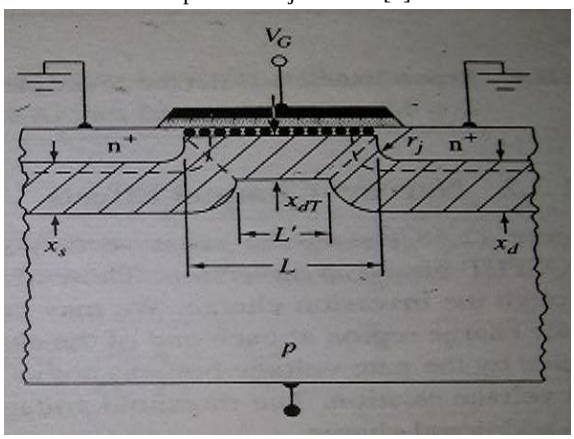

Fig: 2. Charge Sharing in the Short Channel Threshold Voltage Model

Corresponding Author,
E-mail address: er.abikumarec@gmail.com

As the channel length decreases, the threshold voltage shifts in the negative direction. The equation (3) was derived using the assumptions that the source, channel and drain space charge width were all equal. If we apply a drain voltages, the space charge width at the drain terminals widens, which makes channel length smaller, and the amount of bulk charge controlled by the gate voltages decreases. This effect makes the threshold voltage as a function of drain voltage [6].

$$V_{TN} = -\frac{eN_a x_{dT}}{C_{ox}}\left[\frac{r_j}{L}\left(\sqrt{1+\frac{2x_{dT}}{r_j}}-1\right)\right] \quad (3)$$

Where

$$\Delta V_T = \Delta V_{T(short\ channel)} - \Delta V_{T(long\ channel)}$$

S. NO	Voltage	CURRENT		
		I MOSFET (8 microcon)	II MOSFET (16 microcon)	III MOSFET (24 microcon)
1	0v	0	0	0
2	2v	5.5515 x10^{-8} amp	2.5206 x10^{-8} amp	1.6302 x10^{-8} amp
3	5v	2.9576 x10^{-7} amp	1.4617 x10^{-7} amp	9.7072 x10^{-8} amp

S. NO	Voltage	CURRENT		
		I MOSFET (8 microcon)	II MOSFET (16 microcon)	III MOSFET (24 microcon)
1	0v	0	0	0
2	2v	3.7195 x10^{-6} amp	1.7062 x10^{-6} amp	1.09 x10^{-6} amp
3	5v	5.8334 x10^{-6} amp	2.2374 x10^{-6} amp	1.3281 x10^{-6} amp

Table: 1, 2. Comparison between MOSFETs having different channel lengths (8microcon, 16microcon and 24microcon)

We have proposed three MOSFETs with different channel lengths (8 micron, 16 micron and 24 micron). The source and drain regions are doped to 1×10^{19} m^3 electron concentration with n type. While the channel region is doped to 2×10^{14} m^3 electron concentration with p type. The channel width is about 10 micron and the contacts are neutral. The table (1) shows the drain current values at different gate voltage for different channel lengths 8 micron, 16 micron and 24 micron. From the table 1, the first MOSFET (8microcon) has highest drain current as compare to second (16 microcon) and third (24 microcon). So as the channel length increases the drain current decreases with respect to gate source voltage. The fig (3) shows the characteristic curve between gate source voltage and drain current with respect to gate voltage. The I_D versus V_{DS} curve will change with respect to V_{GS} changes. If V_{GS} increases, the initial slope of I_D versus V_{DS} increases. But the value of V_{DS} (saturation) is a function of V_{GS}. The characteristics curve between drain voltage and drain current with respect to drain source voltage is shown in the fig.4. The comparison between threes MOSFETs, which have channel lengths 8microcon, 16microcon and 24microcon as shown in the table-2.

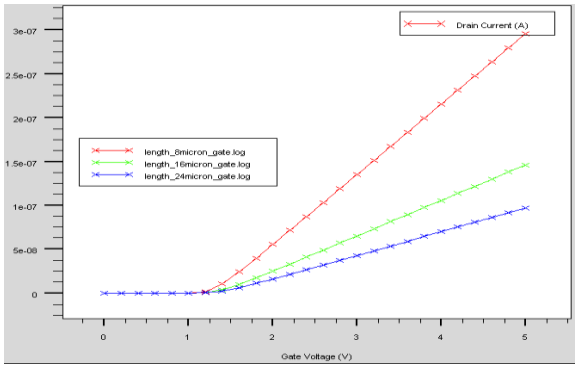

Fig: 3. Characteristics Curve between Gate Source Voltage and Drain Current with respect to Gate Voltage for different Channel Lengths (8 micron, 16 micron and 24 micron)

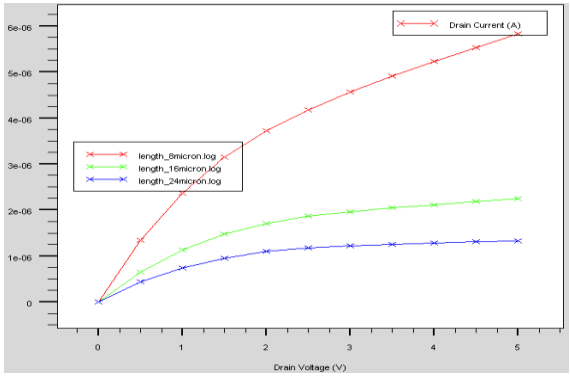

Fig: 4. Characteristics Curve between Drain Current and Drain Voltage with Respect to drain Source Voltage for different Channel length 8 micron, 16 micron and 24 micron

4. Conclusion

A reduction in channel length will increase the trans-conductance and frequency response of the MOSFET, and a reduction in channel width will increase the packing density in an integrated circuit. A reduction in either or channel length and channel width can affect the threshold voltage. Hence as the channel length increased then the slope of I-V characteristics decreased.

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